

R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants thank Examiner Do for the indication of allowable matter in claim 10.

INTERVIEW SUMMARY

Applicants' representative, John Ignatowski, spoke with Examiner Do on May 4, 2005 via telephone. Applicants' representative requested clarification of the rejections for claim 1. The Examiner stated (i) that the reference to FIG. 13 of Zhou should have been to FIG. 2 of Zhou, (ii) the output signal of the A/D circuit 202 of Zhou generates multiple values over time, (iii) the A/D circuit 202 of Zhou inherently has a clock, (iv) the inherent clock for the A/D 202 of Zhou was being used to rejected the claimed "plurality of clock cycles" and (v) clock signals have values of zero or one and thus two clock signals represent a value. No samples were presented. No agreement was reached regarding the claims.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 4 line 20-page 5 line 5 and FIGS. 2-4 as originally filed. Thus, no new matter has been added. As the amendments should only require a cursory review, entry of

the amendments is respectfully requested per M.P.E.P. §714.13 II. If the amendments are not entered, Applicants respectfully request a concise explanation per M.P.E.P. §714.13 III for purposes of a possible appeal.

**OBJECTION UNDER 35 U.S.C. §132**

The objection to claims 1, 11 and 20 under 35 U.S.C. §132 for new matter is respectfully traversed and should be withdrawn.

The text on page 12 line 13-page 13 line 2 and FIG. 3 of the application teaches that each signal LOSFILT1-LOSFILT8 may be set to a loss-of-signal state when an input signal Rx (FIG. 2) is lost for 1-8 consecutive clock cycles, respectively. Thus, each of the signals LOSFILT1-LOSFILT8 may represent a different value of the claimed selected number. The claimed filtering value may be represented by the signal LOSSEL used to address an 8:1 multiplexer 128. In the example provided on page 12 of the application, if the signal LOSSEL has a value of 4, then the signal FLOS (representative of the claimed filtered signal) will be in the loss-of-signal state only after four or more consecutive clock cycles where the input signal is lost. Therefore, the application as originally filed teaches that a filtered signal indicates that an input signal has been lost when the selected number of lost states is greater than a filtering value. As such, the amended

claims 1, 11 and 20 do not contain new matter and the objection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-9 and 11-20 under 35 U.S.C. §102(e) as being anticipated by Zhou has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Zhou discloses a matched filter and signal reception apparatus (Title).

Claim 1 provides a sample circuit configured to (i) detect a state of an input signal and (ii) present a plurality of intermediate signals each representative of the state of the input signal during a plurality of clock cycles. In contrast, the A/D circuit 202 of Zhou (asserted similar to the claimed sample circuit) does not appear to expressly or inherently disclose "sampling with clock" as asserted in the Office Action. In particular, Zhou appears to be expressly silent regarding a sampling clock for the A/D circuit 202. Furthermore, inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). In contrast, Appendix A illustrates that an A/D converter may be implemented without a

clock signal. Per Appendix A, the A/D circuit 202 of Zhou does not necessarily have a sampling clock. Therefore, Zhou does not appear to expressly or inherently disclose or suggest a sample circuit configured to (i) detect a state of an input signal and (ii) present a plurality of intermediate signals each representative of the state of the input signal during a plurality of clock cycles as presently claimed.

Claim 1 further provides a selection circuit configured to present a filtered signal in response to (i) a selected number of the intermediate signals having a lost state and (ii) a multi-bit selection signal representing a filtering value, wherein the filtered signal indicates the input signal has been lost when the selected number of lost states is greater than the filtering value. In contrast, Zhou appears to be silent regarding any value of the A/D circuit 202 representing a "lost state" of the signal Ain (asserted similar to the claimed input signal). Thus, Zhou appears to be silent regarding when a selected number of values in the output signal of the A/D circuit 202 (asserted similar to the claimed intermediate signals) have some undefined lost state. Therefore, Zhou does not appear to teach or suggest a selection circuit configured to present a filtered signal in response to a selected number of the intermediate signals having a lost state as presently claimed.

Assuming, *arguendo*, that the clock signals CLK2 and CLK3 of Zhou define a filtering value (for which Applicants' representative does not necessarily agree), Zhou appears to be silent regarding how a register R21 and a select circuit SEL1 of Zhou (together asserted similar to the claimed selection circuit) determine when the undefined selected number of lost states is greater than the alleged filter value of the clock signals CLK2 and CLK3. In particular, FIG. 2 of Zhou appears to contemplate that (i) the clock signal CLK2 is merely used to instruct the register R21 when to store the output signal from the A/D circuit 202 and (ii) the clock signal CLK3 is merely used to instruct the selection circuit SEL1 to route either the value stored in the register R21 or the register R11 to a circuit XOR1 of Zhou. Nothing in Zhou explains how sampling (R21) and routing (SEL1) compare the undefined selected number of lost states with the alleged filtered value. Claims 11 and 20 provide language similar to claim 1. Therefore, the Examiner is respectfully requested to either (i) clearly identify the number of Zhou allegedly similar to the claimed selected number of lost states and provide a detailed explanation how the register R21 and selection circuit SEL1 of Zhou know when the selected number of lost states is greater than a value allegedly carried by the clock signals CLK2 and CLK3 or (ii) withdraw the rejections to claims 1, 11 and 20.

Claim 11 further provides that the intermediate signals are in parallel. In contrast, the values generated by the A/D circuit 202 of Zhou appear to be sequential. Therefore, Zhou does not appear to disclose or suggest that the intermediate signals are in parallel as presently claimed. Claim 2 provides language similar to claim 11. As such, claims 11 and 2 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 20 further provides a means for detecting a state of an input signal, the state consisting one at a time of (i) a loss-of-signal state and (ii) a signal present state. In contrast, Zhou appears to be silent regarding the output of the A/D circuit 202 (alleged similar to the claimed means for detecting) generating only the loss-of-signal state and a signal present state. Therefore, Zhou does not appear to disclose or suggest a means for detecting a state of an input signal, the state consisting one at a time of (i) a loss-of-signal state and (ii) a signal present state. As such, claim 20 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the sample circuit comprises a detect circuit and a plurality of shift registers. In contrast, Zhou appears to be silent regarding any structure internal to the A/D circuit 202 (asserted similar to the claimed sample circuit). Furthermore, the arguments on page 3 of the Office Action fail to identify where Zhou allegedly discusses the A/D circuit 202

comprising a plurality of shift registers. Claim 12 provides language similar to claim 2. As such, the Examiner is respectfully requested to either (i) clearly identify the shift registers of Zhou allegedly inside the A/D circuit 202 of Zhou or (ii) withdraw the rejections of claims 2 and 12.

Claim 3 provides that the sample circuit comprises (from claim 2) the plurality of shift registers and (from claim 3) a second shift register configured to synchronize the detected signal to a clock signal defining the clock cycles. In contrast, Zhou appears to be silent regarding any express structure within the A/D circuit 202 (asserted similar to the claimed sample circuit). Furthermore, inherency requires certainty of results, not mere possibility. Referring again to Appendix A, an A/D circuit is illustrated without a register to synchronize a detected signal to a clock signal. Therefore, inherency of a second register is not a certainty and *prima facie* anticipation has not been established. Claim 13 provides language similar to claim 3. As such, claims 3 and 13 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 provides that the selection circuit comprises a multiplexer configured to multiplex the second intermediate signals to present the filtered signal **as determined by the multi-bit selection signal**. In contrast, Zhou does not appear to disclose a "multiplexer SELx" as alleged in the Office Action. Therefore,

*prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly identify the SELx circuit of Zhou cited in the Office Action or (ii) withdraw the rejection.

Assuming, *arguendo*, that the Office Action meant that the "multiplexer SELx" was one of the selection circuits SEL1-SELn of Zhou (for which Applicants' representative does not necessarily agree), Zhou appears to be silent regarding any of the selection circuits SEL1-SELn being controlled by the clock signal CLK2 (asserted part of the claimed multi-bit selection signal). Furthermore, Zhou appears to be silent regarding any of the selection circuits SEL1-SELn receiving an output signal from any other selection circuit SEL1-SELn as alleged in the Office Action. Therefore, Zhou does not appear to disclose or suggest a selection circuit comprising a multiplexer configured to multiplex second intermediate signals to present a filtered signal as determined by a multi-bit selection signal as presently claimed. Claim 14 provides language similar to claim 4. As such, the Examiner is respectfully requested to either (i) clearly explain how the selection circuits SEL1-SELn of Zhou multiplex as determined by the clock signal CLK2 (asserted part of the claimed multi-bit selection signal) and how the output of one selection circuit SEL1-SELn is an input to another of the selection circuits SEL1-SELn or (ii) withdrawn the rejections to claims 4 and 14.

Claim 5 provides (from claim 1) that the logic gates receive the intermediate signals from the sample circuit, which the Office Action asserts are generated by the A/D circuit 202 of Zhou. Claim 5 further provides (from claim 4) that the logic gates are configured to present second intermediate signals, which the Office Action asserts are similar to the output of the selection circuit SEL1. Claim 5 further provides that each of the logic gates receive one of the intermediate signals and another one of the second intermediate signals. Despite the assertion in the Office Action, Zhou appears to be silent regarding any circuitry receiving both (i) the output signal from the A/D circuit 202 (asserted similar to the claimed intermediate signal) and (ii) another of the output signals from the selection circuit SEL1 (asserted similar to the claimed second intermediate signal). Furthermore, the assertion on page 3 of the Office Action that the input signal to register R21 is similar to the claimed **second intermediate signals** conflicts with the assertion on page 2 of the Office Action that the input signal to register R21 is similar to the claimed **intermediate signals**. Claim 15 provides language similar to claim 5. Therefore, Zhou does not appear to disclose or suggest a plurality of logic gates (i) receiving intermediate signals from a sample circuit, (ii) configured to present second intermediate signals and (iii) receive one if the intermediate signals and another one of the second intermediate signals as presently

claimed. As such, claims 5 and 15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a second selection circuit configured to present a second filtered signal in response to a second selected number of the intermediate signals having a second predetermined state, the second selected number defined by a second multi-bit selection signal. In contrast, Zhou appears to be silent regarding a second multi-bit selection signal. Therefore, Zhou does not appear to disclose or suggest a second selection circuit configured to present a second filtered signal in response to a second selected number of the intermediate signals having a second predetermined state, the second selected number defined by a second multi-bit selection signal as presently claimed. Claim 16 provides language similar to claim 6. As such, claims 6 and 16 are fully patentable over the cited reference and the refection should be withdrawn.

Claim 7 provides a status circuit configured to present a status signal indicating one of (i) a signal lost and (ii) a signal present in response to both the filtered signal and the second filtered signal. In contrast, Zhou appears to be silent regarding a signal Aout (asserted similar to the claimed status signal) indicating one of a signal lost and a signal present. Therefore, Zhou does not appear to disclose or suggest a status circuit configured to present a status signal indicating one of (i)

a signal lost and (ii) a signal present to in response to both a filtered signal and a second filtered signal as presently claimed. Claim 17 provides language similar to claim 7. As such, claims 7 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides that the selected number and the second selected number are programmable. In contrast, Zhou appears to be silent regarding any values being programmable. Furthermore, the Office Action merely states "e.g., CLK3" for both the claimed selected number and the claimed second selected number. One of ordinary skill in the art would not appear to understand a signal clock signal as anticipating two programmable selection numbers. Furthermore, the Office Action asserts that the clock signal CLK3 of Zhou carries part of a filtering value, not a selected number. Therefore, *prima facie* anticipation has not been established. Claim 18 provides language similar to claim 8. As such, the rejections of claims 8 and 18 should be withdrawn.

Claim 9 provides that the selected number of intermediate signals has a value different than the second selected number of intermediate signals. In contrast, Zhou appears to be silent regarding any two numbers related to the output signal of the A/D circuit 202 (asserted similar to the claimed intermediate signals) are different than each other. Furthermore, the assertion that an XOR function of Zhou causes the unidentified selected number and

unidentified second selected number to be different suggests that the claimed selected number and the claimed second selected number are somehow inputs into the XOR1-XORn circuits in FIG. 13 of Zhou. In contrast, the right input signal into the XOR1 circuit of Zhou is already alleged on page 3 of the Office Action to be similar to the claimed second intermediate signals. The left input to the XOR1 circuit of Zhou appear to be a spread code. One of ordinary skill in the art would not appear to understand a spread code to be similar to either a selected number of intermediate signals having a lost state (from claim 1) or a second selected number of the intermediate signals having a second predetermined state (from claim 6). Therefore, *prima facie* anticipation has not been established. Claim 19 provides language similar to claim 9. As such, the rejections of claims 9 and 19 should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit  
Account No. 12-2252.

Respectfully submitted,

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Dated: May 31, 2005

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Docket No.: 01-349 / 1496.00141

*Appendix A*

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# MICROELECTRONICS

Digital and Analog  
Circuits and Systems

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*Analysis*

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## *Appendix A*

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### MICROELECTRONICS: Digital and Analog Circuits and Systems

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Prefa  
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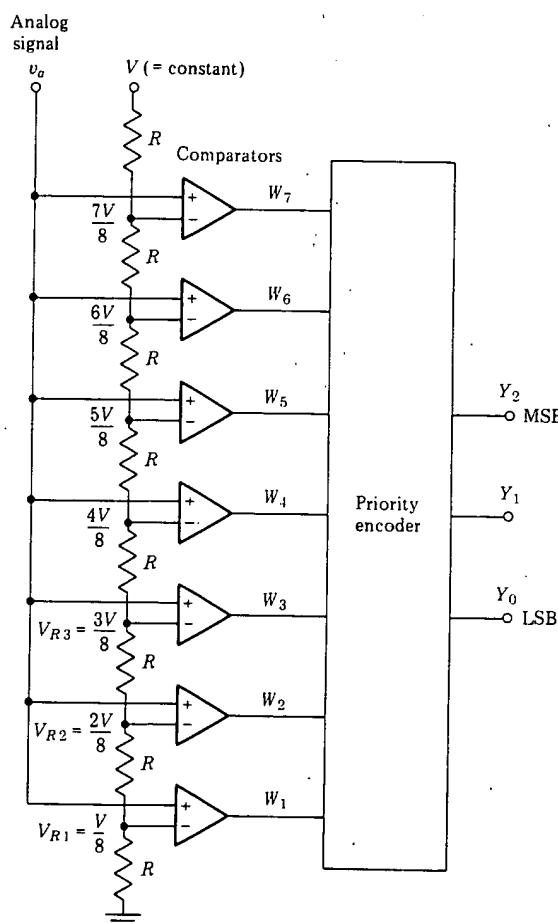
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A-Z

other bits to 0, and the comparator compares the D/A output with the analog signal. If the D/A output is larger, the 1 is removed from the MSB, and it is tried in the next most significant bit. If the analog input is larger, the 1 remains in that bit. Thus a 1 is tried in each bit of the D/A decoder until, at the end of the process, the binary equivalent of the analog signal is obtained. For an  $N$ -bit system, the conversion time is  $N$  clock periods as opposed to a worst case of  $2^N$  pulse intervals for the counting-type A/D converter. The AD7570 (Analog Devices Co.), which is a 28-pin dual-in-line CMOS package, is an 8-bit A/D converter which makes use of the successive-approximation technique.

## The Parallel-Comparator A/D Converter

This system is by far the fastest of all converters. Its operation is easily understood if reference is made to the 3-bit A/D converter of Fig. 16-44. The



**Figure 16-44** A 3-bit parallel-comparator A/D converter.

Sec. 16-13

Table 16-2 The truth table

$W_7$	$W_6$	$W_5$
0	0	0
0	0	0
0	0	0
0	0	0
0	0	0
0	0	1
0	1	1
1	1	1

analog voltage  $v_a$  is applied to equally spaced thresholds. This type of processing is sorted into a given voltage of two adjacent comparators. A very distinctive pattern: low if  $v_a$  is above the input voltage and the threshold is below the analog voltage between  $\frac{1}{2}W_1$  and  $W_1 = 1$ ,  $W_2 = 1$ , and all other values should be 2 ( $Y_2 = 0$ ,  $Y_1 = 1$ ). The output of the first comparator is 1 if the

Conversion time is limited by the priority encoder. Using an 8-to-3 priority encoder and a TI-147 priority-encoder driver, conversion times of 100 ns have been obtained.

An obvious drawback  
The number of comparator  
bits (seven comparators f  
number of comparators a  
larger the  $N$ , the more com

### Dual-Slope or Ratiometric

This widely used system is with  $V_a > 0$  and  $V_R < 0$ . ] cleared. Then at  $t = t_1$ ,  $S_1$  sampled (and hence consta

A-3

D/A output with the analog word from the MSB, and it is input is larger, the 1 remains in decoder until, at the end of final is obtained. For an  $N$ -bit opposed to a worst case of  $2^N$  converter. The AD7570 (Analog I<sup>S</sup> package, is an 8-bit A/D maximization technique.

ters. Its operation is easily converter of Fig. 16-44. The

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Table 16-2 The truth table for the A/D converter of Fig. 16-44

Inputs							Outputs		
$W_7$	$W_6$	$W_5$	$W_4$	$W_3$	$W_2$	$W_1$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

analog voltage  $v_a$  is applied simultaneously to a bank of comparators with equally spaced thresholds (reference voltages  $V_{R1} = V/8$ ,  $V_{R2} = 2V/8$ , etc.). This type of processing is called *bin conversion*, because the analog input is sorted into a given voltage range or "voltage bin" determined by the thresholds of two adjacent comparators. Note that the comparator outputs  $W$  take on a very distinctive pattern: low output (logic 0) for all comparators with thresholds *above* the input voltage and high output (logic 1) for each comparator whose threshold is *below* the analog input. For example, if  $\frac{2}{8}V < v_a < \frac{3}{8}V$ , then  $W_1 = 1$ ,  $W_2 = 1$ , and all other  $W$ 's are 0. For this situation the digital output should be 2 ( $Y_2 = 0$ ,  $Y_1 = 1$ ,  $Y_0 = 0$ ), which is interpreted to mean an input analog voltage between  $\frac{2}{8}V$  and  $\frac{3}{8}V$ .

The truth table with inputs  $W$  and outputs  $Y$  is given in Table 16-2. A comparison with Table 6-3 shows that the logic is that of a 3-bit priority encoder. The  $X$ 's in Table 6-3 are all replaced by 1s. The column labeled  $W_0$  in Table 6-3 is missing in Table 16-2 because, if  $v_a < \frac{1}{8}V$  then  $W_1$  through  $W_7$  are all 0, and the output is zero ( $Y_2 = 0$ ,  $Y_1 = 0$ ,  $Y_0 = 0$ ).

Conversion time is limited only by the speed of the comparator and of the priority encoder. Using an Advanced Micro Devices AMD 686A comparator and a TI-147 priority-encoder conversion, delays of the order of 20 ns can be obtained.

An obvious drawback of this technique is the complexity of the hardware. The number of comparators needed is  $2^N - 1$ , where  $N$  is the desired number of bits (seven comparators for the 3-bit converter of Fig. 16-44). Hence, the number of comparators approximately doubles for each added bit. Also the larger the  $N$ , the more complex is the priority encoder.

### Dual-Slope or Ratiometric A/D Converter

This widely used system is depicted in Fig. 16-45. Consider unipolar operation with  $V_a > 0$  and  $V_R < 0$ . Initially  $S_1$  is open,  $S_2$  is closed, and the counter is cleared. Then at  $t = t_1$ ,  $S_1$  connects  $V_a$  to the integrator and  $S_2$  opens. The sampled (and hence constant) analog voltage  $V_a$  is now integrated for a fixed

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Figure 16-44 A 3-bit parallel-comparator A/D converter.